PAPER

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Computational logic with square rings of nanomagnets

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Abstract

Nanomagnets are a promising low-power alternative to traditional computing. However, the successful implementation of nanomagnets in logic gates has been hindered so far by a lack of reliability. Here, we present a novel design with dipolar-coupled nanomagnets arranged on a square lattice to (i) support transfer of information and (ii) perform logic operations. We introduce a thermal protocol, using thermally active nanomagnets as a means to perform computation. Within this scheme, the nanomagnets are initialized by a global magnetic field and thermally relax on raising the temperature with a resistive heater. We demonstrate error-free transfer of information in chains of up to 19 square rings and we show a high level of reliability with successful gate operations of ~94% across more than 2000 logic gates. Finally, we present a functionally complete prototype NAND/NOR logic gate that could be implemented for advanced logic operations. Here we support our experiments with simulations of the thermally averaged output and determine the optimal gate parameters. Our approach provides a new pathway to a long standing problem concerning reliability in the use of nanomagnets for computation.

Supplementary material for this article is available online

Keywords: nanomagnetism, thermally active nanomagnets, dipolar coupling, Boolean algebra, computation, Boolean logic

(Some figures may appear in colour only in the online journal)

1. Introduction

A non-volatile building block that does not require any standby power, and has low operating power, would be ideal for computing. A particularly promising approach for the design of such a building block is based on nanomagnets, which have a magnetization that can be switched between two stable states that can act as binary bits (corresponding to on and off operation of a traditional transistor) [1–6]. In fact, propagation of information encoded in the magnetic states of a linear chain of dipolar-coupled nanomagnets has recently been demonstrated at the picosecond timescale, indicating that nanomagnet circuits have the possibility to compete with traditional CMOS in terms of operational speed [7]. However, at present, applying nanomagnets to computation faces a number of challenges, including: (i) preparing interconnects that can support transfer of information across a given distance between different computational units and (ii) realizing a reliable computational building block that performs Boolean algebra.

Different approaches to implementing computation using nanomagnets include the spin Hall effect [8], strain induced switching [9] and perpendicular magnetic logic [10–12]. In addition, a variety of fabrication techniques have gained

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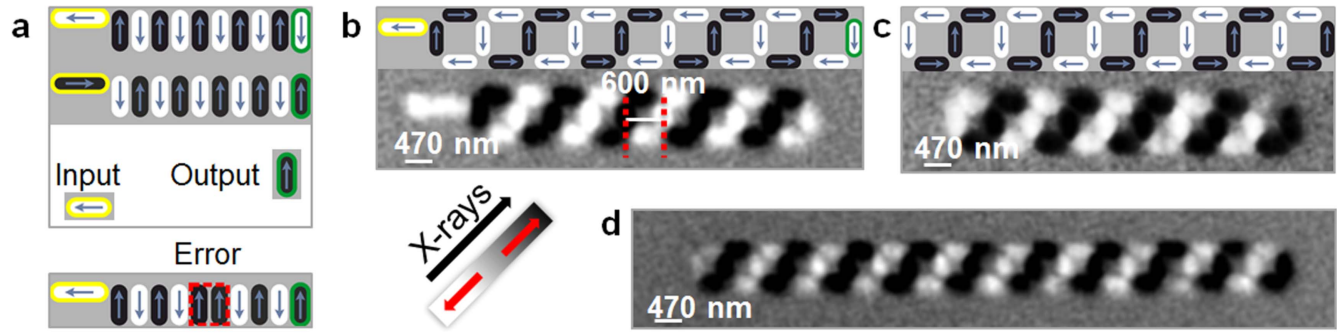

Figure 1. Transfer of information using chains. (a) Schematics of linear chains with input nanomagnets (in yellow) and output nanomagnets (in green). The upper panel displays successful transfer of information, which is encoded in the magnetic states of the input nanomagnets and transferred through antiparallel alignment of the magnetic moments of adjacent nanomagnets (blue arrows). The lower panel demonstrates the appearance of errors (red dashed frame) leading to failure in the information transfer. Schematics and X-PEEM images of a chain of square rings (b) with and (c) without an input nanomagnet (in yellow). The output nanomagnet is in green. (d) X-PEEM image of the longest error-free chain of square rings we have imaged (19 square rings).

attention in the field of nanomagnetic logic in recent years. These include, focused electron beam induced deposition (FEBID) [13–15] and nanostencil lithography [16]. For example, it was recently demonstrated that the coercivity in nanomagnets fabricated using FEBID can be fine-tuned to achieve better device performance [17]. In the current work, we employ thermally-active dipolar-coupled Permalloy ($Ni_{80}Fe_{20}$) fabricated by electron beam lithography.

Up to now, designs of nanomagnets for information transfer have consisted of dipolar-coupled nanomagnets arranged in a chain [2, 18] as shown in figure 1(a). In such a scheme, the shape anisotropy dictates that the magnetic moments are parallel to the nanomagnet long axis and the neighboring nanomagnets in the chain are coupled with opposing magnetic moments due to their interaction via magnetic stray fields. Defining an 'input' nanomagnet, which can be either in state '1' or '0' (upper panel of figure 1(a), shown in yellow), determines the state of the *N*th 'output' nanomagnet (upper panel of figure 1(a), shown in green). However, experimentally such information transfer has so far been limited to chains consisting of a few nanomagnets, where at some distance away from the input magnet—the error-free chain length—the first magnetic error occurs (parallel alignment between neighboring nanomagnets, lower panel in figure 1(a)), introducing uncorrectable errors in the information transfer.

To counter issues with reliability, altering the shape of nanomagnets away from the standard stadium-shaped nanomagnets have been proposed [19, 20]. For example, an additional hard axis was introduced in the nanomagnets that serves as an energy barrier to mitigate external influences such as fluctuations in temperature and surface roughness [21]. Additionally, nanomagnets have been proposed for the realization of logic gate designs involving Boolean algebra [2, 18, 22]. However, similar to the chains, these devices suffer from erroneous operation. With an operating efficiency of 25%–50%—corresponding to the percentage of gates with correct outputs—logic gates using nanomagnets have not been able to compete with existing technology.

In the current work, we implemented a novel nanomagnetic logic design in the form of square ring structures for both information transfer and to perform logic operations. For information transfer, comparing chains of square rings (figures 1(b)–(d) and scanning electron microscope (SEM) image in supplementary figure S1(a), which is available online at stacks.iop.org/NANO/29/265205/mmedia) with linear chains (figure 1(a)), the closure of magnetic flux in a single square ring is supported by two additional horizontal nanomagnets. Within each square ring, the head-to-tail arrangement of nanomagnets, which can be either clockwise or counter clockwise, corresponds to a stable lowest-energy state. For a chain of square rings, the lowest-energy state comprising alternating clockwise and counter clockwise loops is therefore less susceptible to magnetic errors. Indeed, with this design and the application of a dedicated thermal protocol, we have observed that the error-free transfer length is improved compared to previous work where the nanomagnets were not shape engineered [2, 18, 22]. It should be noted that chains containing 19 square rings were the longest we tested, but we expect that much longer error-free transfer lengths can be realized. In a next step, we constructed rudimentary logic gates (figure 2(b)) to demonstrate the feasibility of performing Boolean operations in a reliable manner using the square rings. We contend that our proposed design provides an important step forward for the implementation of nanomagnets in logic circuits to perform computation.

2. Methods

The magnetic nanostructures were fabricated from a Permalloy wedge film on a silicon substrate using electron beam lithography. The nanomagnets have a length $L = 470$ nm, width $W = 200$ nm, and the distance between the centers of two neighboring parallel magnets $a = 600$ nm (see figure 1(b)), which are similar to the dimensions of nanomagnets employed in our previous work [23, 24]. Scalability of the nanomagnets to smaller sizes is feasible [25, 26], with the smallest nanomagnet dimensions limited by the

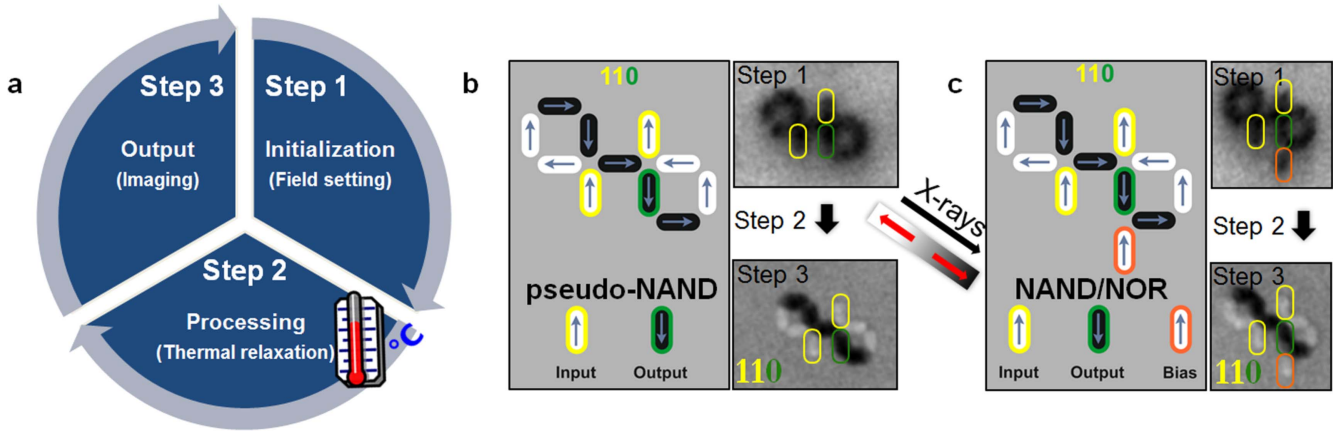

Figure 2. Logic using nanomagnet ring structures. (a) Schematic of the process cycle for logic operation starting with a global field, which sets the direction of all the magnetic moments (Step 1). This is followed by a thermal relaxation to the lowest-energy state (Step 2) and finally the outcome of a successful gate operation (Step 3). (b) A schematic of the pseudo-NAND gate shown along with X-PEEM images of the gate in operation. (c) Full NAND gate operation is obtained by biasing the output of the pseudo-NAND gate with an additional nanomagnet (in orange). The moment orientation of the bias determines if the gate functions as a NAND gate (moment down) or a NOR gate (moment up).

fabrication methods employed. The thickness of the Permalloy film ranged from 1–15 nm over a distance of 3 mm, with a 2 nm thick aluminum capping layer. Both Permalloy and aluminum thin films were deposited in a thermal evaporator at a base pressure of 2×10^{-6} mbar. The magnetic configuration of the nanomagnets is determined predominantly by the shape anisotropy and thus the magnetic moments can only point in one of two directions parallel to the magnet long axis. For the chains of nanomagnets, input nanomagnets (figure 1(b), shown in yellow) were implemented to control the magnetic state and have dimensions of 1 μm $\times$ 200 nm. The larger size provides a higher energy barrier to switching than for the other nanomagnets in the array to ensure that the input nanomagnet maintains the orientation of its magnetic moment throughout the applied thermal protocol, which allows thermal relaxation of the other nanomagnets to the lowest energy state. The thermal protocol is based on our previous experiments on arrays of dipolar-coupled nanomagnets with ultra-low thickness ($\sim$3 nm), where thermally induced moment reorientations are accessible at room temperature [24]. Imaging of the magnetic configurations was performed using x-ray photoemission electron microscopy (X-PEEM) at the SIM beamline, Swiss Light Source of the Paul Scherrer Institute [27], making use of the resonant x-ray magnetic circular dichroism effect at the Fe L_3 edge, which results in a magnetization and helicity dependent intensity of the nanomagnets. Magnetic contrast maps are obtained by pixel-wise division of two X-PEEM images recorded with circularly polarized x-rays of opposite helicity. Bright and dark contrasts indicate moment orientations in the nanomagnets as shown in figure 1. While other techniques, such as magnetic force microscopy [2, 18] and transmission electron microscopy [28], could be used to probe the magnetic configuration of the nanomagnets, X-PEEM has the advantage that one can track the evolution of the magnetic state of several nanomagnet arrays simultaneously and with high magnetic contrast.

3. Results and discussion

We now describe our experiments involving transfer of information in a chain of square rings and a schematic of the process cycle is shown in figure 2(a). First, the input state for the chains is set at room temperature, using a global magnetic field to set the state of the nanomagnets so that all horizontal nanomagnets have their moments pointing to the left and all the vertical nanomagnets have their moments pointing down (Step 1, figure 2(a)). Then, the system is heated to a temperature at which the moments within the chain become thermally active so that their moments can spontaneously switch (for a nanomagnet with a thickness of $\sim$3.0 nm, the activation temperature is $\sim$70 °C). Since the input nanomagnet has an energy barrier that is higher than that of the nanomagnets in the rest of the chain, it does not become thermally active during the thermal protocol and thus defines the resulting output state of the system (Step 2, figure 2(a)). Following thermal activation, the chains of nanomagnets relax to a minimum energy state that is compatible with the orientation of the input nanomagnet while cooling the sample down to room temperature. In particular, the input nanomagnet, which is thermally stable and acts as an encoding source, determines the alignment of the moment in the neighboring magnet. This, in turn, determines the chirality of the moments in the neighboring square ring, which circulate clockwise (anticlockwise) when the magnetization in the input magnet points to the left (right). This establishes the (alternating) chirality of the square rings along the chain of thermally active square building blocks, which finally determines the magnetic state of the output nanomagnet (shown in green in figure 1(b)) in the most distant ring (Step 3, figure 2(a)). Chains with opposite chirality starting from the left are shown in figures 1(c) and (d), this time without an input nanomagnet. We have tested a total of 40 chains consisting of 4, 9, 14 and 19 square rings in two identical samples and observed a yield (total number of defect free chains when compared to total

number of chains) of 100%, 70%, 60% and 50% with increasing chain length. The drop in yield with increase in chain length correlates with the amount of time required for each chain to reach its minimum energy state. Therefore, a longer time (or higher temperature) during the course of the thermal protocol would lead to a higher yield of defect-free chains, as has been demonstrated for large arrays of square rings [23]. The largest chain of square rings where we observed an error-free transfer of information consists of 19 square rings and, with a lattice constant of 600 nm, this corresponds to a propagation length of 11.4 μm (figure 1(d)).

To test the viability of ring structures for use in computation, we built logic gates with the design shown in figure 2(b), which we name a pseudo-NAND gate (an SEM image of the pseudo-NAND gate is shown in supplementary figure S1(b)). Each gate comprises two inputs (ii) and an output (o) defining the logic operation (iio), in which each 'i' and 'o' can be either zero or unity reflecting the moment orientation (down or up, respectively) of the input and output nanomagnets. In a functionally complete NAND logic gate with two inputs, the logic operations are (001), (110), (101) and (011) and in a functionally complete NOR logic gate, the logic operations are (001), (110), (100) and (010). Using the same protocol as for the chains (figure 2(a)), the states of the two input nanomagnets can be set by the direction of the initially applied external field to (00) or (11), and the state of the output nanomagnet is measured after the thermal protocol. Such a procedure was initially performed on a sample containing 48 individual logic gates where we observed that 46 of the gates displayed the correct logic operation. The two failures can be attributed to factors such as surface roughness, variation in nanomagnet shape and microstructural differences. The asymmetry in the design associated with the logic gates means that a global field protocol to set the input nanomagnets would favor the degenerate state involving the logic gate operation of (110) over the (001) logic gate operation (additional details are found in supplementary figure S6). One way to access the other degenerate state is to incorporate long nanomagnets as inputs so that they remain stable across the thermal protocol. An example of a logic operation of (001) performed by a logic gate with long input magnets is shown in supplementary figure S7. To statistically validate the operational reliability of our gates, we fabricated and tested a second sample containing 3630 gates. A map of the logic gate failures is shown in figure 3, in which each 'pixel' corresponds to 11 logic gates and their associated color indicates the number of failed logic gates. The error map demonstrates an operational window encompassing 2310 gates at thicknesses between ~2.2 and 4.5 nm where logic operations involving nanomagnets are expected to perform optimally, resulting in either the state (110) or (001). In summary, we experimentally observe a success of ~94%, as shown with 'red diamond' markers on the plot in figure 4(a).

In order to gain insight into the operation of the considered logic gates, a simplified model system is considered. In particular, each nanomagnet is approximated by a point-dipole, which interacts with all other point-dipoles via the

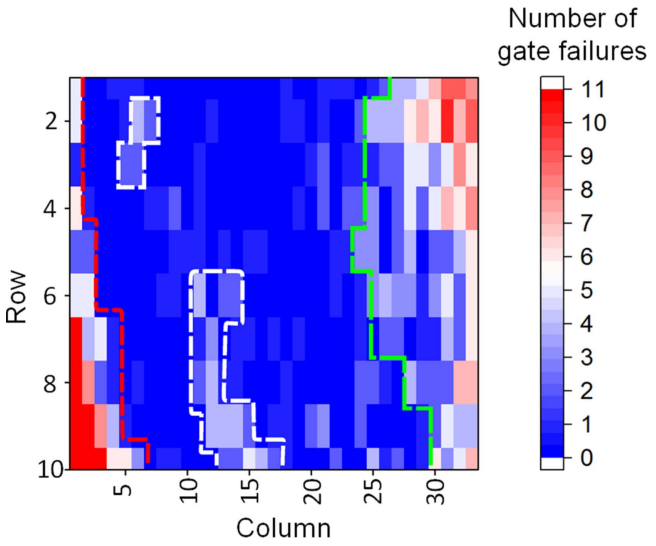

Figure 3. Map of logic gate failures. Logic gates are in a grid pattern where column values correspond to (approximately) varying thickness. Each 'pixel' in the plot corresponds to 11 logic gates and is color coded based on the total number of logic gate failures. Higher (lower) values of columns are associated with thinner (thicker) regions. Logic gate failures agree well with the variation in thickness of logic gates across the sample. The optimal operation of the gates, where the thermal activation energy of the nanomagnets is neither too high nor too low, is found in a thickness window between ~2.2 and ~4.5 nm. Thicker regions, consisting of nanomagnets with a higher thermal activation energy, and therefore frozen moments, are to the left of the red dashed line and thinner regions, consisting of nanomagnets with low thermal activation energy, and therefore moments fluctuating at timescales shorter than the measurement time, are to the right of the green dashed line. There are regions shown with a white dashed frame within the operational window where we observed increased errors, which are likely to be related to defects in the sample.

dipolar interaction:

$$V(r_{ij}, m_i, m_j) = -\left(\frac{\mu_0}{4\pi r_{ij}^3}\right)[3(m_i.\hat{r}_{ij})(m_j.\hat{r}_{ij}) - m_i.m_j],$$

where r_{ij} is the distance vector separating the ith and jth moments, m_i and m_j. The total energy of the system is therefore given by:

$$E_{\text{total}} = \frac{1}{2}\sum_{i,j=1}^{N} V(r_{ij}, m_i, m_j).$$

Here N is the number of nanomagnets in a considered logic gate. The dipole moment of each nanomagnet is given by the product $M_s LWd$ where M_s is the magnetization at saturation, L is the length, W is the width and d is the thickness of the nanomagnets. For the current simulations, we used values of $L = 470$ nm, $W = 200$ nm and $a = 600$ nm, as in the experiment, with a thickness $d = 3$ nm and M_s ranging between 200 and 800 kA m^{-1}. Such a point dipolar approximation is found to describe the energetics and kinetics of the experimental system [24].

To calculate the thermal average of a given nanomagnet subject to chosen inputs, the discrete energy spectrum for a logic gate is first calculated. This gives the energies of the

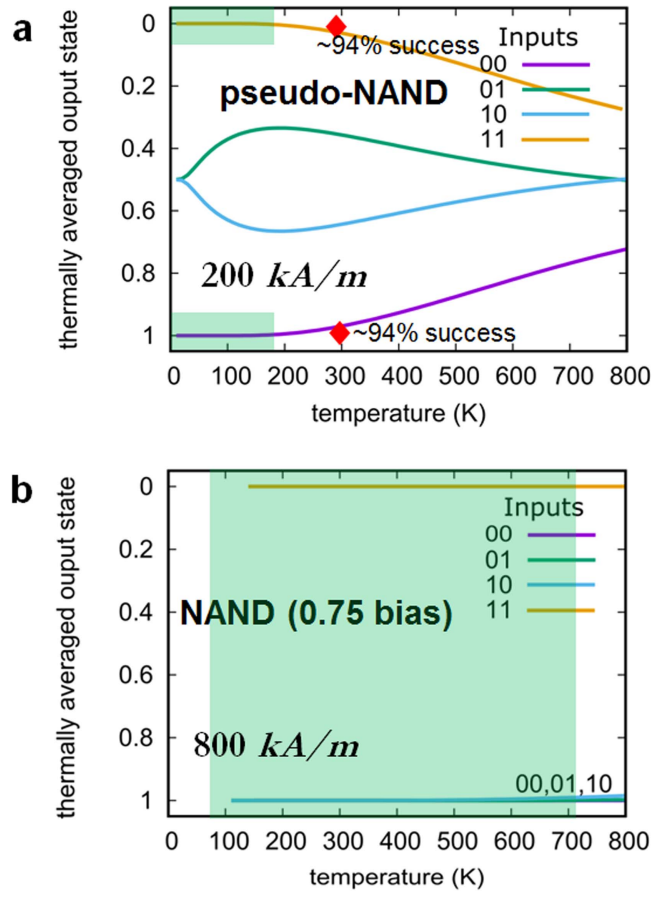

Figure 4. Simulated performance of pseudo-NAND and NAND gates as a function of temperature. (a) Thermally averaged output of a pseudo-NAND gate. The lines are simulated data. The red diamonds are the experimental data for gate operations of (001) and (110). (b) Thermally averaged output of a functionally complete NAND gate with M_s (gate) = 800 kA m^{-1} and M_s (bias) = 600 kA m^{-1}. The green shaded regions indicate the temperature range where the gates are expected to be fully reliable (only for operations of (110) and (001) for the pseudo-NAND gate).

states, $E_1 \ldots E_M$, where $M = 2^N$ is the total number of states admitted by the system. The thermal average for all the gate operations involving inputs of (00), (11), (10) and (01) are calculated within the framework of statistical mechanics using the reduced partition function: $Z = \prod_i^{M'} e_i^{-E_i/k_BT}$, where M' is the total number of gate operations for the chosen input constraints.

In the simulation, when we consider an $M_s = 200$ kA m^{-1} for all nanomagnets in the pseudo-NAND gate, we find that the gate operations of (110) and (001) are stable for temperatures <200 K (giving thermally averaged outputs of 0 and 1, respectively) and the operations involving inputs of (10) and (01) show thermally averaged outputs of ~0.6 and ~0.4, respectively (see supplementary figure S2(a) and schematic of all possible pseudo-NAND logic operations shown in supplementary figure S4). Upon increasing the M_s to 800 kA m^{-1}, we find that the gate operations of (110) and (001) are now stable for temperatures of up to 800 K and the gate operations involving inputs of (10) and (01) yield a thermally averaged output of ~0.5 (supplementary figure S2(b)). Therefore our simulations show that, on increasing M_s, the gate operations of (110) and (001) are stable at higher temperatures[6]. However, the failure of gate operations (101) and (011) in the pseudo-NAND design implies that it does not in its current form fulfill the NAND logic truth table and thus cannot be considered as a functionally complete NAND logic gate.

In order, therefore, to create a functionally complete NAND logic gate, a bias nanomagnet can be added to the design (see figure 2(c), SEM image in figure S1(c), and schematic of all possible NAND logic operations in supplementary figure S5). Depending on the orientation of the magnetic moment in the bias nanomagnet, either a NAND or NOR gate can be constructed (moment pointing down or up, respectively). The simulations for $M_s = 200$ kA m^{-1} demonstrate that logic gates with the new design now perform all the NAND gate operations, i.e. (11), (00), (01) and (10) input operations give thermally averaged outputs of 0, 1, 1 and 1 for temperatures <50 K (supplementary figure S2(c)). In order to access correct gate operations at room temperature, we increase the M_s and find that a value of 800 kA m^{-1} leads to a failure probability of 10^{-2} (supplementary figure S2(d)). The failure probability can be significantly lowered by lowering the M_s of the bias nanomagnet expressed as a bias factor, $b = \frac{M_s(\text{bias})}{M_s(\text{gate})}$. With M_s (gate) = 800 kA m^{-1}, and for $b = 0.75$ (M_s (bias) = 600 kA m^{-1}), we obtain a failure probability of $\sim 10^{-5}$ at room temperature (figure 4(b) and supplementary figure S3(b)), thus improving the reliability of the NAND gate by a factor of $\sim 10^3$, and we expect the same improvement in reliability for the NOR gate. Further lowering of the failure probability, in order to directly compete with CMOS [29], may be obtained by increasing the magnetization of each nanomagnet either by increasing the volume of the nanomagnets or by using a magnetic material with a higher magnetization. The failure probability was determined for the input operation of (10), since it sets the baseline of failure probability for the entire NAND gate (supplementary figure S2(d)), as it is the only output that varies with temperature. When we compare simulation results from the pseudo-NAND gate and NAND gate (figure 4), we can deduce that an experimentally realized NAND (and NOR) gate would operate with high success similar to our pseudo-NAND gate, since the experimentally observed success of logic gate operations agrees well with the simulation (red diamonds in figure 4). We include results from a NAND/NOR design test (figure 2(c)) that incorporated a bias nanomagnet with the same M_s as all other nanomagnets in the design. Within the operational thickness window, corresponding to a total of 210 NAND/NOR logic gates, we observed that >90% of the gates performed a successful logic gate operation involving inputs of (11) and (00). Device realization of either the NAND or NOR gate can be achieved through a variety of means to set the moment of the bias nanomagnet in a specified direction, for example, with a current carrying nanowire providing a local Oersted field or by coupling the

[6] Note that we experimentally observed an almost zero failure probability for gate operations of (110) and (001) at room temperature. A comparison of this result with figures S2(a) and S2(b), implies that the experimental M_s is larger than 200 kA m^{-1}.

(ferromagnetic) bias nanomagnet to an antiferromagnetic layer to enforce exchange bias.

4. Conclusion

We have demonstrated a new approach to computation with nanomagnets arranged in square rings, which has the potential to support information transfer across varying distances and perform logic operations with high success. While the current work utilizes a thermal protocol to allow the nanomagnets to relax to the lowest energy-state, this relaxation may be performed by other means, for example using a magnetic field-protocol [2], all-optical switching [30] or thermal relaxation induced by laser pulses [31], and reducing power consumption by operating the devices close to the Landauer limit [6]. The increased reliability additionally opens up opportunities to explore other avenues of computation that do not involve the standard Boolean schemes [32, 33].

Acknowledgments

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